Thermal management and characterization of flip chip BGA packages

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Thermal Management and Characterization of Flip Chip BGA Packages

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Abstract

This paper presents the various types of thermally enhanced flip chip packages and its thermal characterization with thermal management options at package level. The conventional one-piece lid high performance flip chip BGA package (HP-fcBGA) has its strength in good thermal dissipation capability, however its board level solder joint reliability could be comprised due to the direct contact of the one-piece metal lid with the substrate. By encapsulating the flip chip with molding compound leaving the die top exposed, a planner top surface can be formed. And a flat lid can then be mounted on the planer mold/die top surface. In this way the direct interaction of metal lid with the substrate can be removed. The new extra performance flip chip BGA package (XP-fcBGA) is thus less rigid under thermal loading and solder joint reliability enhancement is expected. A third option of flip chip package XPs-fcBGA (with a dummy die between flip chip and metal lid as spacer) has been explored by UTAC for the solution of taller-than-flip-chip decoupling capacitors. This paper examines the thermal performance of XP-fcBGA and XPs-fcBGA packages versus the HP-fcBGA design. A series of experimental and computational studies were conducted to obtain the thermal resistance under JEDEC still and forced air (1m/s, 2m/s and 3m/s) environmental conditions. Experimental data of HP-fcBGA and XP-fcBGA recorded a thermal resistance θja 8.89deg.C/W and 8.86deg.C/W at zero airflow respectively, achieving good correlation with simulation results. Correlation within 10% range was also obtained for forced convection conditions of 1m/s, 2m/s and 3m/s airflow. Slight degradation in thermal performance of XPs-fcBGA was observed. Proper selection on the dummy die size is deemed necessary.

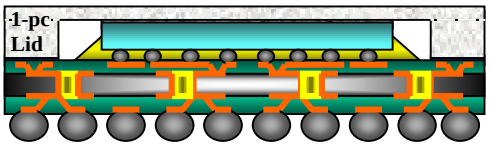
Keywords: Flip chip, thermal resistance, CFD modeling and simulation, thermal measurement and thermal performance.

Nomenclature

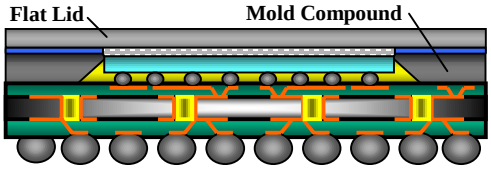
Q	= Total power, W
θja	= Junction to ambient thermal resistance, deg.C/W
θjth	= Thermal resistance, deg.C/W
Tj	= Junction temperature, deg.C
Ta	= Ambient temperature, deg.C
Tc	= Package case temperature, deg.C
K	= Thermal conductivity, W/mK

1. Introduction

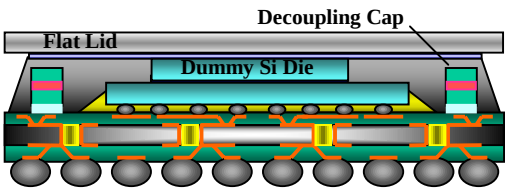
The flip chip BGA package has shown significant interest among the electronic packaging industry in this decade due to its high I/O count and power dissipation capability. Moreover, the advancement in IC package development is continuously driven by the increase of transistor density and clock speed in the chip. In general an IC package merits relate to IC density, excellent electrical performance, high power capacity and efficient heat dissipation capability. The flip chip interconnect technology coupling with heat spreader attachment has emerged as a popular package solution for higher pin count and superior heat dissipation. Efficient thermal applications of the high-performance flip chip BGA (HP-fcBGA, Fig. 1a) and extra-performance flip chip BGA (XP-fcBGA, Fig. 1b - patent pending) have been developed by UTAC [1-2]. In these two configurations in ease of heat removal from the flip chip, a metal heat spreader is attached on the top of the package. Optimum metal thickness was determined for the betterment of thermal management at package level. Hence, the die junction temperature can be maintained at a minimum level. Moreover the heat spreader acts as an environmental protection to the die.



a) HP-fcBGA Package.



b) XP-fcBGA Package (Patent Pending).



c) XPs-fcBGA Package.

Fig 1. Three Different Designs of Thermally Enhanced Flip-Chip BGA Packages.

With the one-piece lid attached to the HP-fcBGA package, it has resulted in a lower level of solder joint reliability during thermal cycling test due to restricted flexing in the package [2]. It was shown that with the elimination of the direct interaction between the metal lid and substrate, the XP-fcBGA package has become less rigid and thus resulted in a higher solder joint fatigue life. With the increase in IC functioning speed and frequency, the issue of power integrity has become more important and complex. Decoupling capacitors are usually placed near the active ICs for an improvement in the power distribution system. In some cases, the decoupling capacitors are taller than the flip chip. This has resulted in the difficulty of forming a planer surface for the lid attachment in the XP-fcBGA design. Thus the option of stacking a dummy metal conductive material as spacer (usually made silicon die) on the flip chip has been implemented to increase the mold thickness (as shown in Fig. 1c). The new structure is termed as XPs-fcBGA. The XPs-fcBGA design poses some process assembly and material usage challenges. Incoming customer wafers may vary in chip thickness, thus resulted in the use of different dummy die thickness in order to meet consistent overall package height. As the use of silicon die as a dummy conductive material is costly, an optimised silicon die size needs to be determined for cost reduction with no compromise in heat dissipation effectiveness.

This paper presents the various thermal management options available at package level for the flip chip BGA package. Series of experimental and computational studies were performed to obtain the thermal management solutions. Thermal test vehicles of size 40x40mm with ball count of 1521 were built. The HP-fcBGA and XP-fcBGA packages were mounted onto a 4-layer PCB (based on JESD 51-9 standard) and underwent experimental measurements at still and forced air environments (1m/s, 2m/s and 3m/s) to obtain the junction to ambient thermal resistance value (θ_{JA}). Finite element modeling method was employed to study the thermal performance across the different flip chip package structures.

2. Thermal Perspective of HP-fcBGA and XP-fcBGA

In a conventional flip chip package, the flip chip die is bonded to the substrate with solder bump interconnects. Active surface of the die (i.e. heat source region) is located near the interconnects. Underfill material is filled in between the die and substrate to relief the thermo-mechanical stresses of the solder bumps due to the CTE mismatch between the silicon die and the substrate. The one-piece heat spreader attached in the HP-fcBGA is shown in Fig. 2. In either the HP-fcBGA or XP-fcBGA design with the metal lid attached on the top surface of the die, considerable portion of the heat will be dissipated on the package top. Therefore the primary heat paths of the packages are from die to package top and bottom collectively. Fig. 3 depicts the heat flow path and thermal resistances from the die to external environment (air). Heat removal is possible in all three modes of heat transfer (conduction, convection and radiation). In one way considerable heat is transferred to the PCB from the chip via the substrate and solder balls. In other way, heat is removed from the die top to the metal lid.

Fig 2. 40x40mm Copper Heat Spreader of HP-fcBGA.

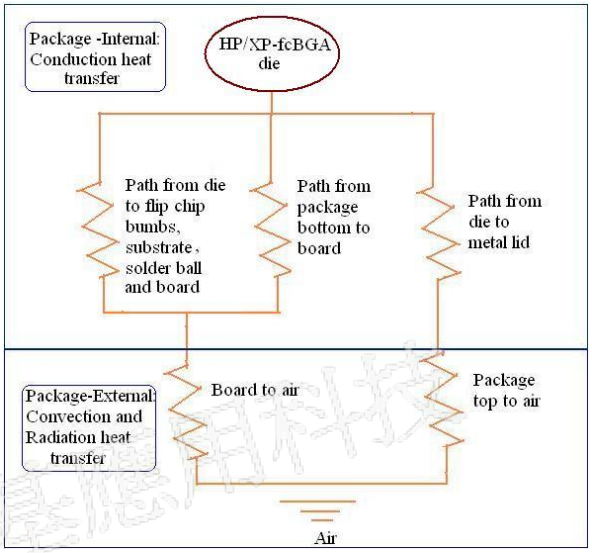


Fig 3. Heat Flow Path and Thermal Resistance from Die to External Environment (air) for the Flip Chip Packages.

The new XP-fcBGA package is similar to conventional HP-fcBGA package with the exception of the heat spreader attached to the mold compound surface instead of the substrate. Total number of solder balls (ball count) is 1521 for both package designs. The physical dimensions are body size of 40x40 mm, flip chip die size of 12x12x0.65mm and bump count of 3500. An eight-layer BT substrate used for simulation and experiments. A 0.5mm thick flat metal lid (made of copper) is mounted over the XP-fcBGA package with a thermally conductive epoxy. Package components and their thermal properties are given in the Table 1.

Within the pacakge, heat transfer in the form of conduction is involved. To impove the heat conduction, good heat conduction path is made from die to the package top surface by a heat spreader. As far as convection heat transfer is concerned, convective heat transfer co-effiecent acts as a vital role and can be improved by increasing the air velocity. In most of the air cooled devices, radiation effects are minimal and can be ignored. In general, conduction and convection equation can be written as follow:

$$Q = \Delta T / R \qquad (1)$$

In this equation R is the combination of all parts of the thermal resistance in the package where

$$R = L/KA \text{ or } 1/hA \qquad (2)$$

L is the length, A is the cross-sectional area, K is the thermal conductivity, & h is the coefficient of heat transfer. The package thermal budget is usually defined by the maximum junction temperature, power dissipation, and ambient conditions. These three factors are often combined as a single parameter known as Theta Ja (θja), where it is the junction-to-air thermal resistance. This is defined by the temperature difference between the die junction and the ambient divided by the total power dissipated.

Table 1.Material Properties of HP/XP-fcBGA.

Details	Description	Thermal Conductivity, W/mK
Package	Mold compound	0.99
	Substrate die-electric (BT)	0.377
	Solder mask	0.25
	Solder ball	50.9
	Chip (die and dummy die)	117.5-0.42x(T-100)
PCB	PCB dielectric	0.3
	Cu trace	385
Metal lid/ heat spreader	Cu	385
Metal lid adhesive	For HP-fcBGA	0.4
Metal lid adhesive	For XP-fcBGA	2.5

3. Thermal Charaterization (Resistance)

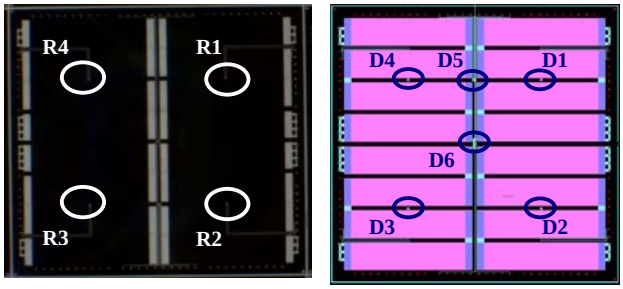
IC packages can normally be ranked by its thermal characterization parameter i.e., θja, θjc& θjb and can generally be defined as

$$\theta jth = \Delta T / Q \qquad (3)$$

where θjth = thermal resistance (θja, θjb or θjc), ΔT = Tj-Tr, Tr is the reference temperature (can be of ambient temperature Ta, board temperature Tb, or package case temperature Tc). And Q is the steady state heat dissipation (or power) of the package.

4. Experimental Test Cases and Methodology

Thermal test vehicles of the HP-fcBGA and XP-fcBGA packages were built with a thermal die of 12x12x0.65mm. The built-in heating resistors and sensing diodes provided the heating of the die and sensing of the die junction temperature respectively (see Fig. 4). Temperature sensing diodes were placed in proximity to the hot spot points in the die. Parallel resistance circuit was made in a such way to heat up the die as shown in Fig. 5.



a) Heating Resistors b) Sensing Diodes

Fig 4. Locations for Heating Resistors and Sensing Diodes on Thermal Test Die.

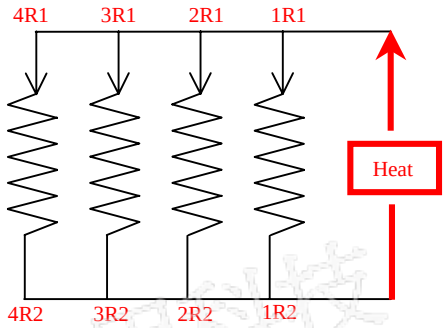


Fig 5. Parallel Resistance Circuit for Die Heating.

The four-wire resistance measurement method was used to eliminate the parasitic resistances as shown in Fig. 6. All the HP and XP-fcBGA packages were mounted onto a Jedec specified 4L board, with the measurement taken at still air condition and forced convections of 1m/s, 2m/s, and 3m/s in a wind tunnel system. For each case, three sample size was used. As per Jedec standard JESD 51-1, junction temperature was measured by the standard Electrical Test Method (ETM) to characterize the package [5].

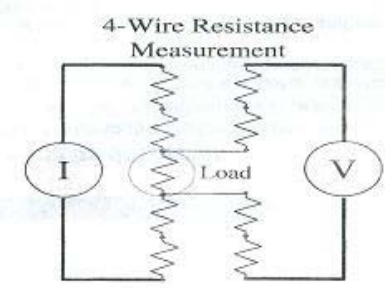


Fig 6. Four-wire Resistance Measurement Method.

For each test vehicle, K factor calibration of the thermal test die has to be conducted in a temperature controlled oven. To find out the K factor listed in equation (4), temperature in the oven was ramped from room temperature to 60deg C, 90 deg C and 120 deg C for calibration.

$$Tj = kV + c \qquad (4)$$

where T is the temperature, k is the slope, V is the sensing voltage and c is the intercept of the curve. For that, a constant sensing current was supplied across the diodes. Sensing voltage and thermocouple reading (case temperature measurement illustrated in Fig. 7) were recorded at steady state room temperature. Steady state is defined by a change of 0.5 deg C in a five minute interval. One sample calibration of the HP-fcBGA package is shown in Graph 1. As shown, the two diodes were calibrated for accurate thermal measurement to get the junction temperatures at two different locations i.e., diode 5 (near the die centre, T5) and diode 1 (T1).

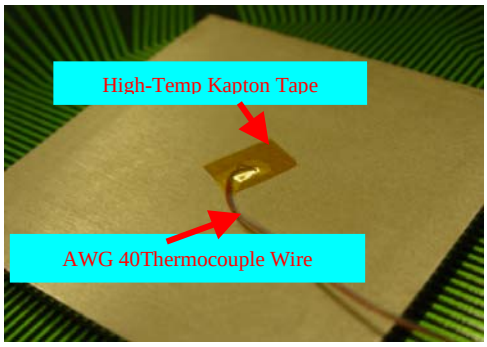
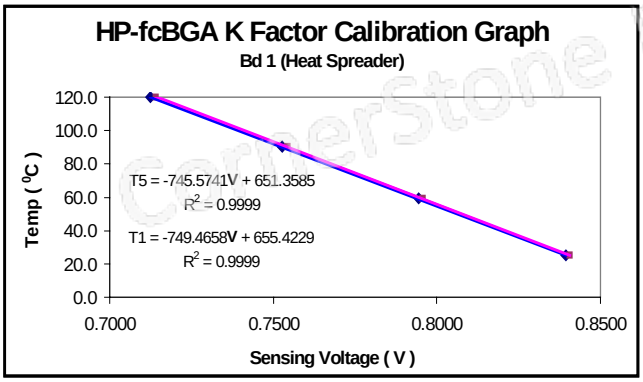


Fig 7. Thermocouple Measurement for Case Temperature.

Graph 1. K Factor Calibration for HP-fcBGA.



After the calibration, actual thermal measurement was performed by injecting a heating power of 10 watts to each test package. Afterwhich the sensing voltage of the diode was monitored for the computation of the junction temperature per equation (4). And thermal resistance of the package will be calculated using equation (3).

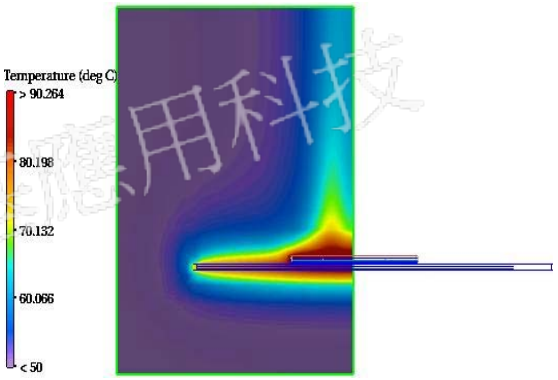
5. CFD Modeling and Simulation

The Flotherm version 4.2, a commercially available finite volume based Computational Fluid Dynamics simulation software, was used to model and simulate the cases of HP-fcBGA and XP-fcBGA packages. The flip chip (die), heat spreader (metal lid) and solder ball were modeled with three-dimensional (3D) elements. The flip chip bumps and heat source were modeled using two-dimensional elements. In this study a 3D laminar flow was used in a convection-free condition with an ambient condition of 25 deg C as given in JESD51.2 [3]. And a 3D turbulent flow was used in a forced convection condition with an ambient of 25 deg C as defined in JESD 51.6 [4] and created in Flotherm v4.2 for package characterization. The common specifications for the simulation model are shown in the Table 2.

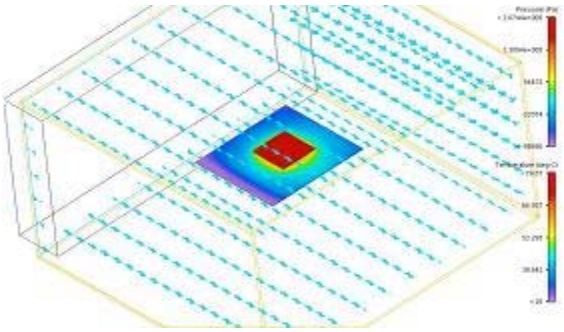
Table 2. Common Specifications for Simulation Models.

Package size	40 x40 mm
Die Size	12x12x0.65 mm
Die power	10 watts
Ambient temperature	25 deg C
Ball pitch	1mm
Total ball count	39x39 (1521)
Total flip chip bumbs	3500
Substrate	8 layer BT

Fig. 8 shows the Flotherm post processing images for still air and force air simulations.



a) Qurter Model - Still Air Condition.



b) Forced Air Condition.

Fig 8. Air Flow Images for Still and Forced Air Conditions.

6. Results and Discussions

6.1 CFD Model Validation

Main objective of this study is to validate the HP/XP-fcBGA finite element models. A comparison of

computationally predicted and measured junction temperatures for the packages mounted onto a 4L PCB board with 0m/s, 1m/s, 2m/s and 3m/s airflow conditions at the ambient temperature of 25 deg C are shown in Tables 3 & 4 and Graphs 2 & 3. Table 3 / Graph 2 and Table 4 / Graph 3 display the results for HP-fcBGA and XP-fcBGA packages respectively. It can be seen from Graphs 2 & 3 that the junction temperatures predicted by simulation fall within a 10% error range when compared to the measured values. The 10% range is widely accepted as a criteria by the industry, thus the accuracy of the CFD models is valid.

Table 3. Measured and Simulation Results Correlation for HP-fcBGA Package.

Wind Speed	Simulated		Measured (Temp Sensor 5)		%Error (Temp Sensor 5)	
m/s	Tj (°C)	Theta ja	Tj (°C)	Theta ja	Tj (°C)	Theta ja
0	113.6	8.86	114.54	8.89	0.83	0.34
1	92.3	6.73	95.82	7.31	3.86	7.93
2	83.1	5.81	87.03	6.41	4.75	9.36
3	77.7	5.27	78.85	5.59	1.49	5.72

Graph 2. Validation of HP-fcBGA Thermal Resistance.

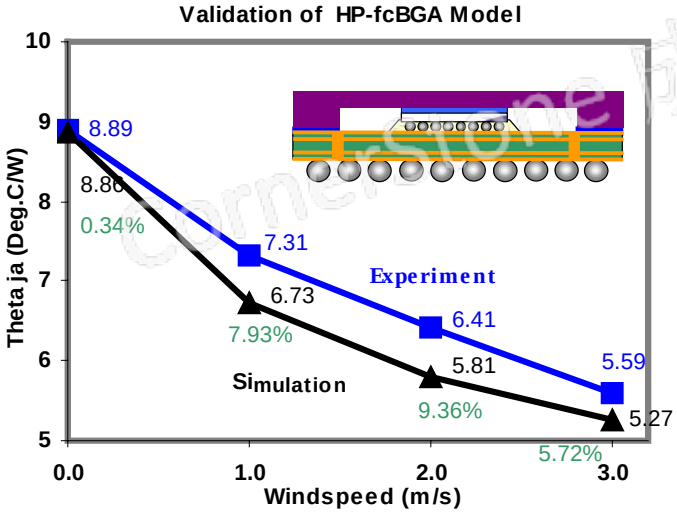
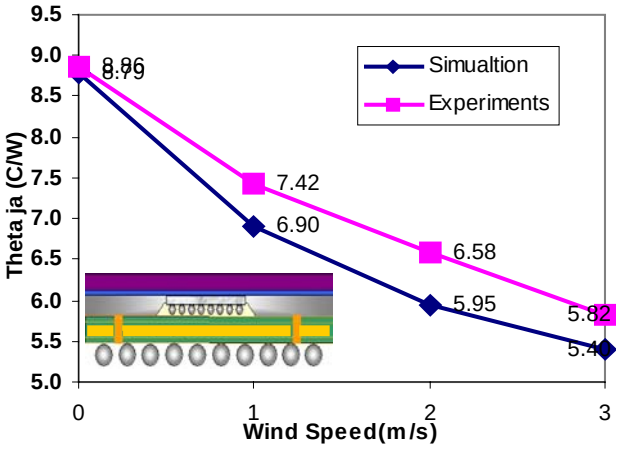


Table 4. Measured and Simulation Results Correlation for XP-fcBGA Package.

Wind Speed (m/s)	Simualtion Theta ja(C/W)	Measurement Theta ja (C/W)			Average Theta ja(C/W)	%error between Simulation & Measurement
		Board A	Board B	Board C		
0	8.79	9.12	8.80	8.66	8.86	0.79
1	6.90	7.63	7.21	7.42	7.42	7.00
2	5.95	6.76	6.44	6.54	6.58	9.60
3	5.40	6.18	5.53	5.75	5.82	7.22

Graph 3. Validation of XP-fcBGA Thermal Resistance.



6.2 XP-fcBGA with External Heat Sink

A study was made to determine the thermal performance of the XP-fcBGA package with a single dispense of the thermally conductive adhesive (which is usually of a lower stress modulus) instead of a two-step dispense of thermal grease and structural adhesive separately. The advantage of putting an external pin fin heat sink is also being evaluated. Details of the heat sink include size of 40x40mm, fin height of 15mm, base thickness of 1.5mm, fin size of 0.7x0.7mm and array of 11x11. Thermal performance comparison is given in Table 5.

Table 5. Thermal Performance Comparison for XP-fcBGA Package.

	Thermal Resistance, Theta ja (°C/W)			
Windspeed (m/s)	HP-fcBGA	XP-fcBGA	XP-fcBGA (low stress adhe)	XP-fcBGA (with heat sink)
0	8.86	8.79	8.75	5.84
1	6.73	6.90	6.90	3.47
2	5.81	5.95	5.77	2.62
3	5.27	5.40	5.26	2.29

From the above results it illustrated that the use of a single dispense thermally conductive adhesive does not affect its thermal performance. Package junction temperature has to be within the limiting temperature irrespective of high power application and stringent environmental condition. Hence there would be situations where thermal management solution is necessary such as using of an extended heat sink. Modeling result showed that with a pin fin type heat sink mounted, a 33% reduction in θ_{JA} can be achieved at zero windspeed condition.

6.3 Sensitivity Study of Spacer Die in XPs-fcBGA

In the development of the XPs-fcBGA package, some challenges were encountered in the process assembly and material usage concern. Multiple flip chip thickness will be needed to mount onto the package based on different

Table 6. Thermal Performance Comparison for XPs-fcBGA Packages.

a). Thickness: Flip Chip = 0.52mm, Dummy Die = 0.44mm.

	Thermal resistance theta Ja (deg C/W)					% thermal degradation (wrt XP-fcBGA)			
Speed	XP-fcBGA	XPs-fcBGA(A)	XPs-fcBGA(A)-16.2x12.2 mm	XPs-fcBGA (A)-8.2x6.2 mm	XPs-fcBGA(A)-5.3x3.3 mm	XPs-fcBGA (A)	XPs-fcBGA(A)-16.2x12.2 mm	XPs-fcBGA (A)-8.2x6.2 mm	XPs-fcBGA(A)-5.3x3.3 mm
0	8.04	8.24	8.31	8.47	8.59	2.49	3.36	5.35	6.84
1	5.23	5.46	5.51	5.67	5.79	4.40	5.35	8.41	10.70
2	4.43	4.61	4.69	4.84	4.95	4.06	5.87	9.26	11.74
3	3.95	4.14	4.20	4.41	4.49	4.81	6.33	11.65	13.67

b). Thickness: Flip Chip = 0.74mm, Dummy Die = 0.22mm.

	Thermal resistance theta Ja (deg C/W)					% thermal degradation (wrt XP-fcBGA)			
Speed	XP-fcBGA	XPs-fcBGA(B)	XPs-fcBGA (B)-16.2x12.2 mm	XPs-fcBGA (B)-8.2x6.2 mm	XPs-fcBGA (B)-5.3x3.3 mm	XPs-fcBGA (B)	XPs-fcBGA (B)-16.2x12.2 mm	XPs-fcBGA (B)-8.2x6.2 mm	XPs-fcBGA(B)-5.3x3.3 mm
0	8.04	8.10	8.31	8.39	8.44	0.75	3.36	4.35	4.98
1	5.23	5.45	5.48	5.57	5.61	4.21	4.78	6.50	7.27
2	4.43	4.61	4.67	4.74	4.78	4.06	5.42	6.99	7.90
3	3.95	4.13	4.18	4.51	4.48	4.56	5.82	14.18	13.72

customers' requirements. It would be cost economical to use the same mold chase to assemble parts with different flip chip thickness. Thus a feasible solution would be to mount a spacer die of suitable thickness on top of the flip chip to match the mold chase thickness. The present solution uses dummy silicon die as spacer that is costly. An optimised silicon die size should thus be determined for cost reduction with no compromise in heat dissipation effectiveness. The basic model of XP-fcBGA was used to build the XPs-fcBGA packages in Flotherm to study their thermal performance. A series of thermal simulation was performed for XPs-fcBGA of different configurations; A) flip chip and dummy die thickness of 0.52mm and 0.44mm respectively, B) flip chip and dummy die thickness of 0.74mm and 0.22mm respectively. A realistic flip chip size of 16x21mm was used, with dummy die sizes of 16x21, 12.2x16.2, 6.2x8.2 and 3.3x5.3mm being evaluated. The modeling results are reflected in Table 6. It was found that in all environmental conditions, XP-fcBGA's thermal performance is better than the XPs-fcBGA design. Comparable thermal performance was observed for different flip chip thickness (0.52 vs 0.74mm), thus indicating that the use of a common mold chase tool would be feasible without affecting the heat dissipation capability of the XPs-fcBGA package. When the dummy die size reduces, a compromise in heat dissipation ability was observed. Maximum degradation in thermal performance is 6.8% @ still air condition and 13.7% @ 3m/s forced air condition when the dummy die is shrunk from 16x21mm to a minimum of 3.3x5.3mm. Hence appropriate selection of the dummy die size is necessary when cost of the silicon is considered.

7. Conclusion

The following conclusion were drawn from this study: 1) Simulation models validation has been achieved by experimental measurement of the thermal test vehicles of HP-fcBGA and XP-fcBGA mounted on a 4 layer Jedec standard board. 2) Thermal performance of the XP-fcBGA package was analysed for various thermal management options like introducing low stess adhesive and external pin fin heat sink. 3) Sensitivity studies were performed for the XPs-fcBGA design to understand the impact of different flip chip thickness and spacer die sizes on its heat dissipation capability.

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