A COMPLETE GUIDE TO 3D CHIP-PACKAGE THERMAL CO-DESIGN… 10 KEY CONSIDERATIONS

DR JOHN PARRY, CENG
LEE WANG, MBA

WHITEPAPER

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WHY IS CHIP-PACKAGE THERMAL CO-DESIGN IMPORTANT?

Chip-package co-design is important for several reasons. Designing a large high power die, e.g. a System-on-Chip (SoC) without considering how to get the heat out is likely to lead to problems later on, resulting in a sub-optimal packaging solution from cost, size, weight and performance perspectives. Historically IC design has considered the die temperature to be uniform. This is no longer a valid assumption in many cases. Heating due to current leakage, which is temperature dependent, is making power dissipation less uniform, and the use of thinner die, now well below 50µm, has reduced the heat spreading capability of the die itself. Both of these effects contribute to greater on-die temperature variation.

WHEN IS CHIP-PACKAGE THERMAL CO-DESIGN ESSENTIAL?

Chip-package co-design becomes essential when designing multi-die chips such as stacked Three-Dimensional Integrated Circuits (3DICs). The dies cannot be designed independently due to their electrical and thermal interaction. Through Silicon Vias (TSVs) that act as inter-die interconnections can help get heat out of the die stack, although their primary role is in reducing hot spots, so their placement relative to high power regions on the die can have a marked effect on the overall thermal performance. Conductive heat transfer is a highly 3D phenomenon so the package temperature distribution affects the temperature distribution on the die.

Thermal is one of the key challenges preventing 3D becoming a mainstream technology within the semiconductor industry. Other issues are the lack of design tools that fully support 3D design, the need to individually test for known-good die and more complex design-for-test. There are issues with the assembly of material stack with differing thermomechanical properties and handling issues associated with thinned die. High currents through very small vertical connections makes power delivery another challenging area despite the focus on low power designs.

This whitepaper focuses on 3D chip-package co-design. The advanced technologies used in 3D packages mean that traditional approaches to chip design are inadequate, for example using temperature guard bands to ensure the device will operate across the maximum range of operating temperatures, where the temperature is assumed to be uniform throughout the die.

With increased power densities for 3D ICs power dissipation per unit volume at the package level increases. Heat generated within a die stack has to be removed through the die stack. Bonding between the dies increase the die-die thermal resistance while aggressive thinning of the die to fit within the allowable package height reduces the die's ability to spread heat so the lateral thermal resistance is also increased. This coupled with the non-homogeneous distribution of both the 3D electrical connections and heat sources on each of the die means that the traditional power-aware IC design flow is no longer adequate. The IC design flow now needs to be fully thermally-aware, as well, with temperature distribution through the package and its dies predicted throughout the IC design flow.

Mentor has a complete chip-package-system thermal solution enabled by the Project Sahara/FloTHERM integration that provides the unique ability to accurately model a design from the die level to the system level e.g. inside the die, inside the package, and package to system. Very accurate boundary conditions can be imported for more accurate die/package modeling for IC thermal analysis. Similarly, accurate die/package models can be passed outward to the system level for accurate system modeling. To get an understanding of this topic it is helpful to consider the IC design flow in three stages, although in practice these can overlap somewhat.

PACKAGE PRE-SELECTION ACTIVITIES

The first stage is the package selection, aimed simply at choosing the best package for the IC in question.

1: ALWAYS START WITH THE PACKAGE SELECTION

To get the correct temperature distribution within the die, it's essential to include the package construction in the thermal model, mounted on a typical PCB and where appropriate with a representation of a heatsink solution, so that the effect of heat spreading in the board and into the heatsink are accounted for in the predicted temperature distribution throughout the package. For this a full computational fluid dynamics (CFD) simulation is required to correctly predict the way the package interacts thermally with its environment, and hence predict the correct temperature distribution within the package itself.

Note that simply applying a constant thermal resistance value to each surface of the die to represent the heat flow path to the ambient is not sufficient as a boundary condition. A high resistance to the ambient does not capture any local heat spreading effects due to the presence of high thermal conductivity materials that are in close thermal contact with the die itself. These tend to hold the die temperature uniform without contributing significantly to the total thermal resistance to the ambient. Using a single thermal resistance value may lead to over, and possibly incorrect design.

In early design, and before the detailed IC design work starts, there is the greatest scope for optimizing the chip-package architecture. At this stage an initial assumption of the number of dies, and the intended size and budgeted power for each die can be used to create a 3D thermal conduction model (which can also include convection and radiation if the package style includes an internal cavity) of the candidate package(s) that can be used to explore the package design space.

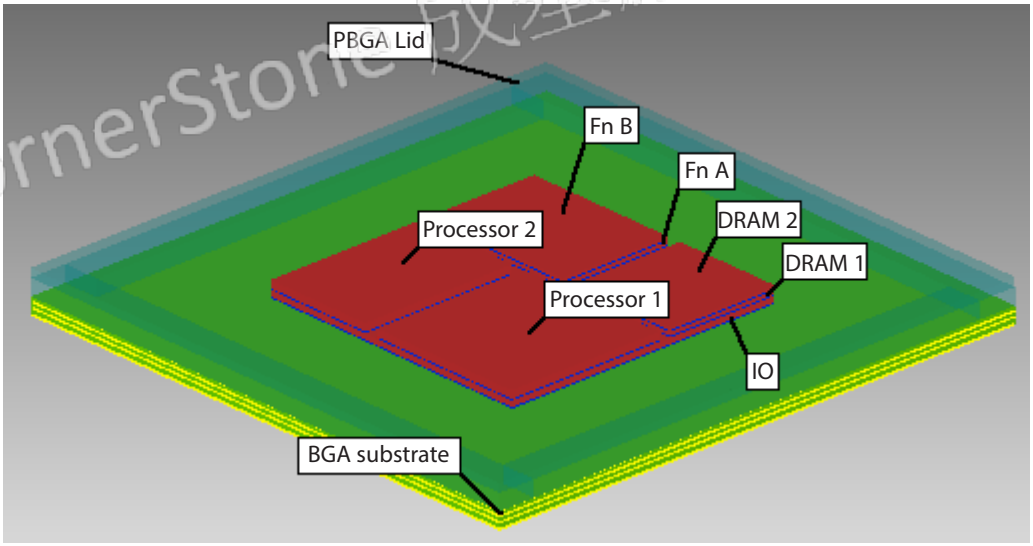

Figure 1: Detailed Thermal Model of a BGA Package With Multiple Die in FloTHERM

2: EXPLORE THE PACKAGE DESIGN SPACE BEFORE THE IC DESIGN STARTS

The thermal model of the candidate package(s) can be used to investigate the influence on the thermal performance of different die arrangements, package size and packaging materials, for example the amount of copper in the substrate for a Ball Grid Array (BGA) package.

At this stage there is a high degree of freedom, and hence opportunity, to explore different package options, and the design of each. Based on an initial estimate for the size of the die, design parameters that can be investigated to determine their influence on the die temperature rise and variation for a given package style may include:

- Influence of the number and possible layout of TSVs
- Influence of the size, shape, and material choices for an interposer
- Effect of interfacial resistances (glue layers)
- Pyramid vs. overhang stack arrangements (if wire bonded)
- Cooling solutions internal to the package, e.g. die edge cooling, internal heat slugs, etc.
- Influence of external cooling solutions, e.g. solder pads, underfill options etc.

Features that have the greatest effect on die temperature rise and variation self-indicate the need to be modelled in greater detail, and optimized for thermal performance.

3: INCLUDE TEMPERATURE DEPENDENT THERMAL PROPERTIES

This is automatic for silicon and other materials included in FloTHERM's material library. Temperature ranges across the die are likely to be too high to assume a single thermal conductivity value, so temperature-dependent thermal conductivities are necessary to accurately predicting die hot spot values. Note that for transient calculations it is essential to include the material density and specific heat capacity. This happens automatically in FloTHERM when a material is attached to an object.

4: REFINE THE DIE SURFACE TREATMENT

Include a 3D representation of the active layers of the die (metallization and polysilicon) with an isotropic block several microns thick.

Silicon dioxide (SiO_2) and silicate glass, typically used as dielectric materials to separate metal wires on the active surface of the die have thermal conductivities of the order of 1 W/mK, around two orders of magnitude less than the metal they isolate, historically being aluminium or copper. Wires on different levels run in different directions, so the material behaviour is locally orthotropic. However, recognising the high level of interconnection between the levels, combined with metal running in different directions, causes the heat to smear. Hence for early design activities outside the main IC design flow the bulk behaviour can be approximated with an isotropic material with all the active surface layers captured within the thickness of one mesh cell in the package-level model.

The IC process and design technology files contain information about metal width and spacing as well as the preferential routing directions. This can be used to calculate the overall thickness and an isotropic averaged material property for this thermally-active layer.

Up to this stage heat should be distributed uniformly over the die. This will not be the case in practice, and the model should be refined to remove this assumption as soon as more detailed information starts to become available from the IC design team. The benefit of using this assumption at the outset is that it gives an indication of the inter-die temperature variation that arises from the package's limited ability to hold the bulk die temperature uniform.

This is quite a lot of work to do before the IC design work starts, but that design effort can tie up a lot of people, so good preparation will ensure these resources are used as efficiently as possible, and the IC design timescale is as compressed as it can be.

EARLY DESIGN DIE-PACKAGE THERMAL EXPLORATION & OPTIMIZATION

Having selected the most promising package from a thermal standpoint and gained an understanding of how the package and die combinations work thermally the package-die co-design work can start. The work at this stage includes 3D partitioning of functionality across the different die, functional block and TSV floor planning for the die, and interface layer design. Hence we are at the start of the process shown in Figure 2, but having already investigated the thermal performance of the candidate package type:

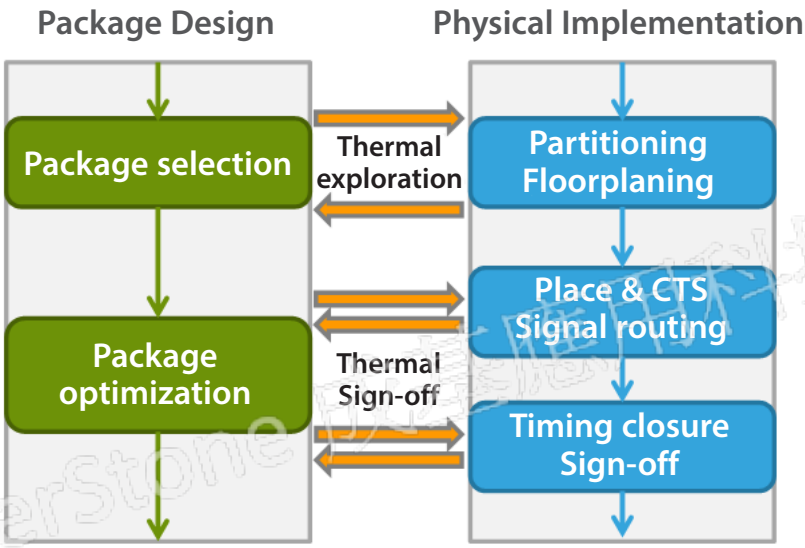

Figure 2: Recommended Package-Die Thermal Design Flow

5: ESTABLISH AN EFFICIENT WORKFLOW

To do the thermal simulations at the package level, it is necessary to get geometry and power dissipation changes from the IC design team and into FloTHERM. Fortunately FloTHERM has FloSCRIPT which records actions taken in the software, which can then be played back so the same steps can be repeated error-free.

This is particularly useful for changes to the model that have to be made again and again over the course of the development, for example the power distribution on each of the die resulting from the current floorplan layout, and the number and distribution of the TSVs through the die to make the necessary die-die electrical connections.

The workflow for the rapid updating of the model can be established during the package pre-selection phase, programmatically deactivating or deleting the original geometry, and loading and positioning the replacement geometry before re-solving the case.

CALIBRE'S TEMPERATURE-AWARE DESIGN FLOW INCORPORATING FloTHERM

6: BACK-ANNOTATE TEMPERATURE INFORMATION BEFORE FLOORPLANNING

Providing the IC design team with information about the average die temperature and temperature variation for each die before the IC design process starts can greatly help floorplanning [Ref. 1]. Floorplanning is critical to the quality of the design, as decisions made during floorplanning can either alleviate or exacerbate this temperature variation. Just like the package pre-selection activities, early IC design aims to explore the design space to come up with the best solution that takes into account the thermal impacts, so lots of ideas have to be assessed quickly.

It is now possible to do fast iterations of the thermal impact of different floorplans that also incorporate the thermal design of the package directly into the IC design flow, as FloTHERM can now be used alongside Mentor's Calibre suite (DESIGNrev & RVE) to simulate a thermal model of the package built within Calibre to give a fully temperature-aware IC design flow, codenamed Project Sahara.

Project Sahara focuses on early design exploration through to final sign-off. A FloTHERM model of a 3DIC can be created by Project Sahara to allow the 3DIC package to be imported into a larger board-level or system-level, to fully account for the effects of the application environment.

7: USE FUNCTIONAL BLOCK POWER BUDGETS DURING FLOORPLANNING

Once floorplanning starts, get a high-level power map from the IC design team and import that into the thermal model of the package.

FloTHERM has a Die SmartPart that allows powers to be read in as a CSV file so this can be done automatically and the results quickly fed back as the simulation model will often only take a matter of minutes to run, indicating where TSVs can be introduced to improve the thermal performance, or where other design changes are needed. For example, it may be important to ensure that two or more different functional blocks operate at very similar temperatures to eliminate timing issues.

8: EXPLORE THROUGH-SILICON VIA LAYOUTS

For logic-on-logic 3DICs this should be accounted for when partitioning the design amongst the various dies, and during inter-die and intra-die floorplanning, requiring power map information for each die.

At this stage opportunities exist to move the functional blocks in both x- and y-directions (xy expansion) keeping their relative positions the same but adjusting the gaps (white space) between them into which TSVs can be inserted to examine their impact on die hot spots. Knowing the TSV size and pitch, which scale with die thickness, blocks of higher through-plane thermal conductivity can be superimposed over the die thickness in these white space regions in FloTHERM, to locally override the properties of silicon.

Optimizing both functional block and TSV layouts during floorplanning is to be done as part of the IC design flow, with thermal as just one of the constraints on that process.

9: MAKE THE IC DESIGN FLOW TEMPERATURE AWARE

As floorplanning progresses, the thermal design effort needs to focus on the detail of the thermal interaction between die as the design is further elaborated. The power map for the die becomes much more detailed, and in the case of a 3DIC, the number and location of TSVs need to be defined as part of the electrical design. Clock tree synthesis (CTS) is a critical step in the IC design flow that has to close before the die can be routed, with the physical timing closure taking into account the placement, clock tree synthesis, and routing, which all have to be timing-aware to get timing closure for modern synchronous IC design.

Since 2012, Mentor has partnered with TSMC to create a thermal analysis flow based on FloTHERM and Calibre DESIGNrev and RVE, an industrial standard physical verification results viewing environment [Ref. 3].

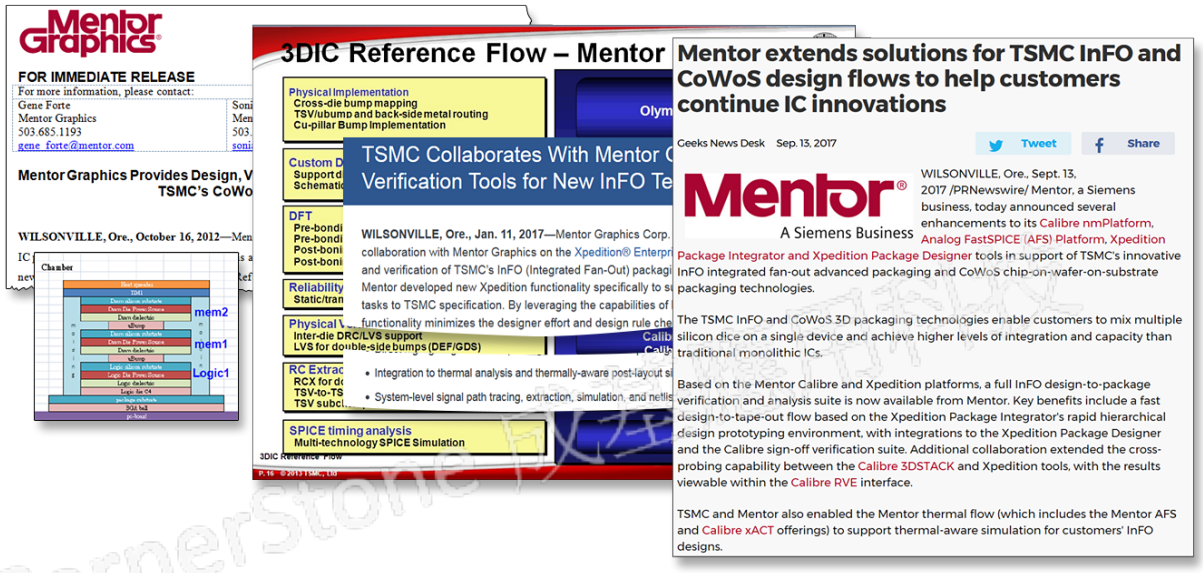

Figure 3: TSMC Reference Flow Collaborations

Project Sahara is essential for this fine detail work needed to get timing closure and sign off the design that is also thermal-aware. It provided an easy-to-use, fast and accurate tool to do thermal simulation on dies and interposers of 3DIC within a full package model, enabled by automatic gridding that is built into this solution that uses a localized grid in critical model areas such as the dies.

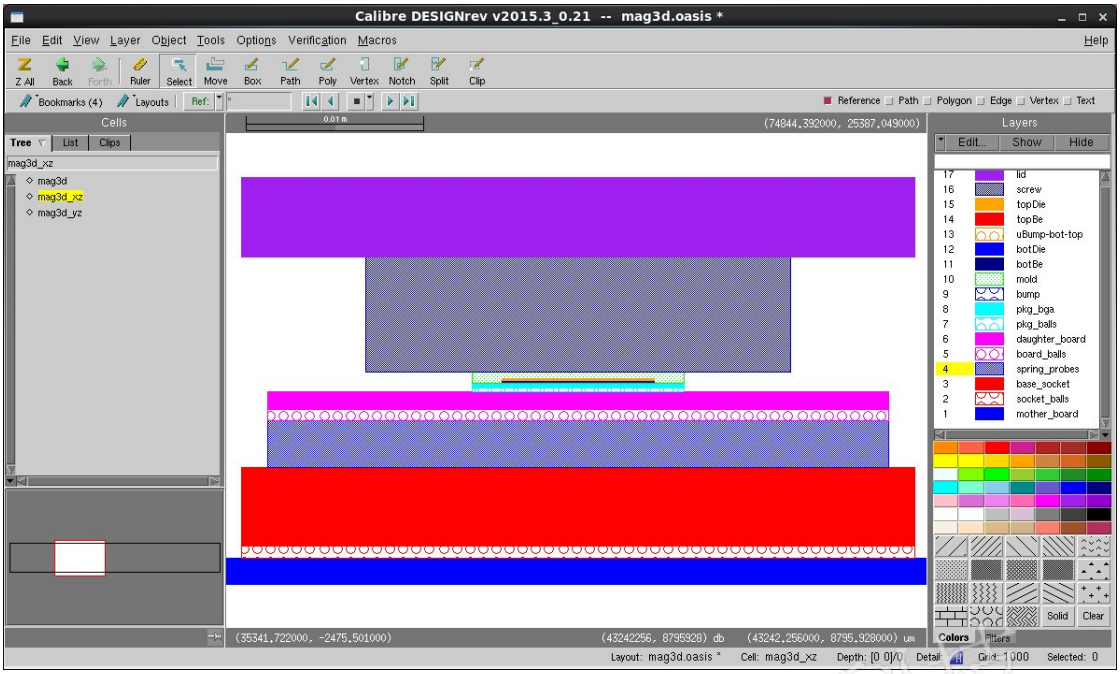

Figure 4: Assembly View of Thermal Model within Calibre DESIGNrev

This solution takes die power map files that can be generated by power analysis tools, and creates thermal maps that can be used for thermal design and for checking against thermal constraints. The thermal results can also be displayed in a histogram in Calibre RVE, and the thermal hotspots highlighted onto the design in Calibre DESIGNrev. In transient analysis, temperature vs. time graphs can be displayed using Mentor Graphics EZwave, a high-capacity, high-performance graphical waveform environment. Power and temperature waveforms can be displayed on the same window and even overlaid for easy correlation.

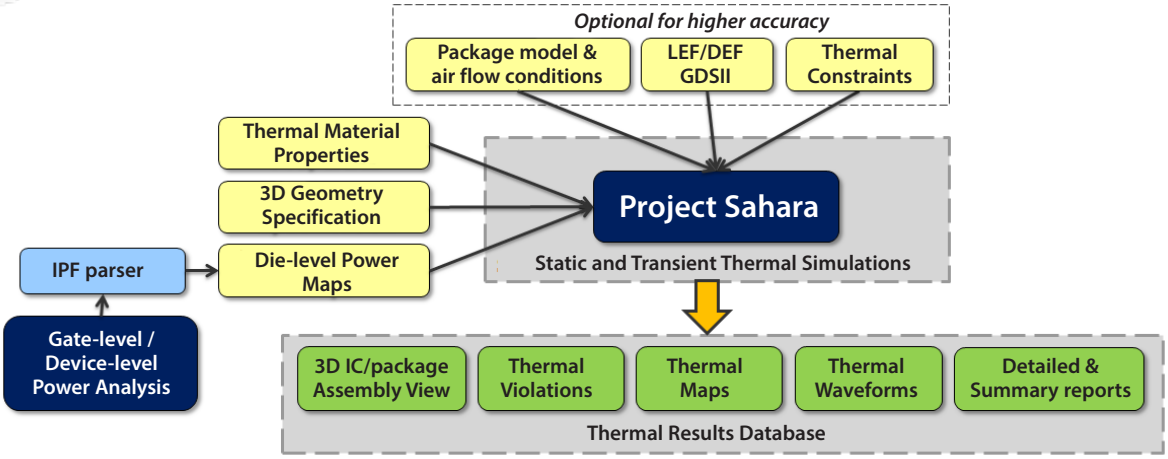

Figure 5: Thermal Modeling Methodology of Project Sahara

Within this flow the thermal model generation and validation, GDSII-based extraction of the thermal properties and Instance Power File (IPF)-based power map generation are done within the Calibre environment. As such the thermal models of dies are more accurate than typically possible to build outside the IC design flow, taken into account the metallization, such as interconnects as well as TSVs within the dies.

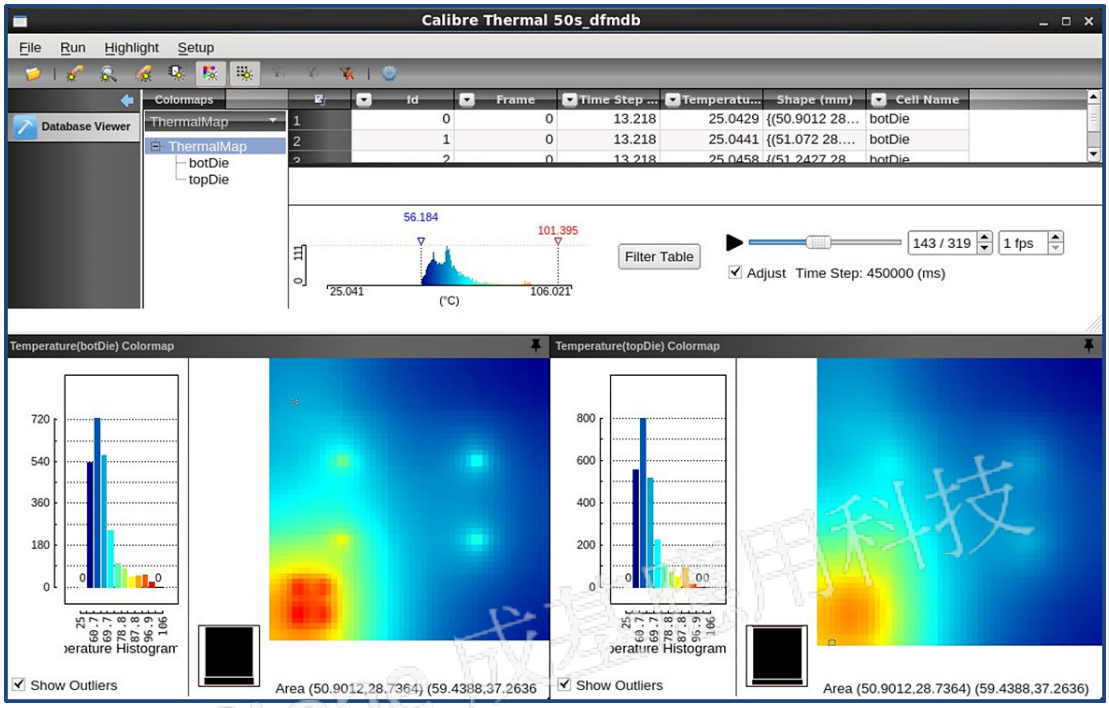

Figure 6: Thermal Colormap and Histograms in Project Sahara

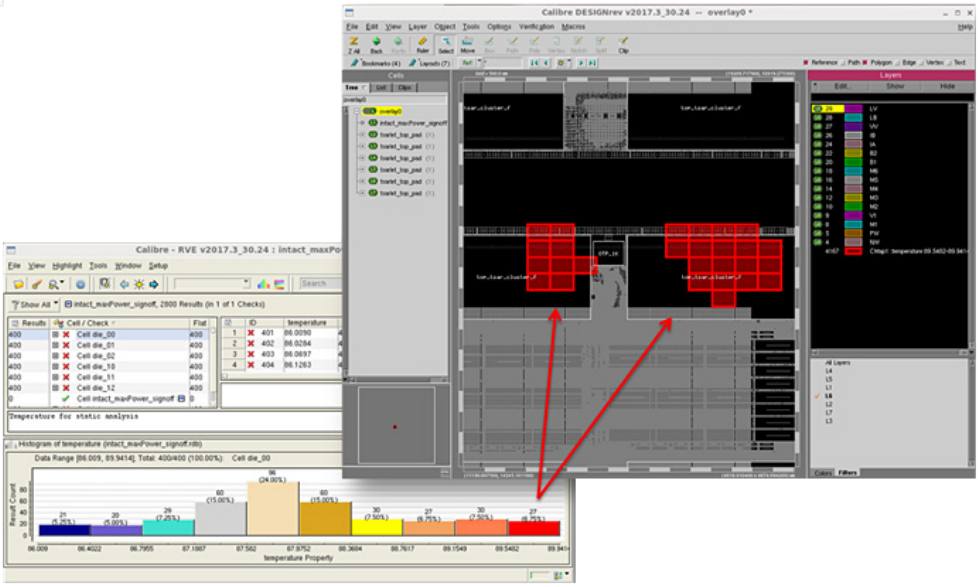

Figure 7: Thermal Histogram in Calibre RVE and Hostpot Overlay in Calibre DESIGNrev

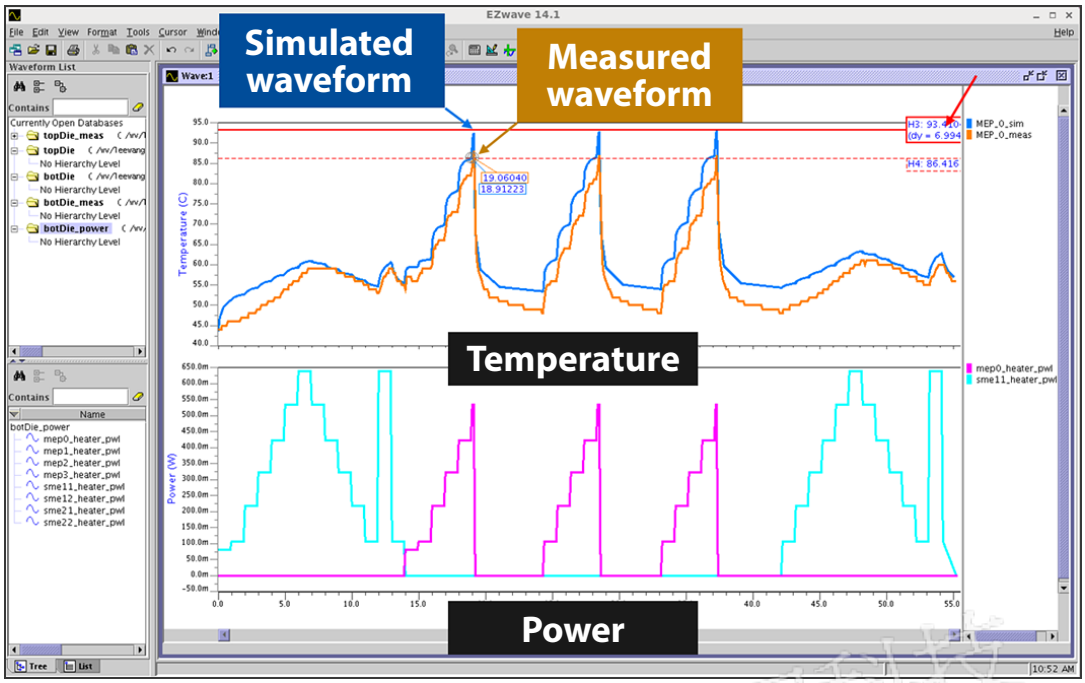

Figure 8: Temperature and Power vs. Time Curves Displayed using Mentor Graphics EZwave

TIMING CLOSURE AND SIGNOFF

10. USE ACCURATE DIE-LEVEL THERMAL ANALYSIS

While performing a complete chip-package-system thermal simulation fine-grain details can be accounted for by automatically computing the equivalent anisotropic thermal properties by extraction from the layout. As the focus shifts towards getting timing closure and signoff the granularity of the extraction can be increased.

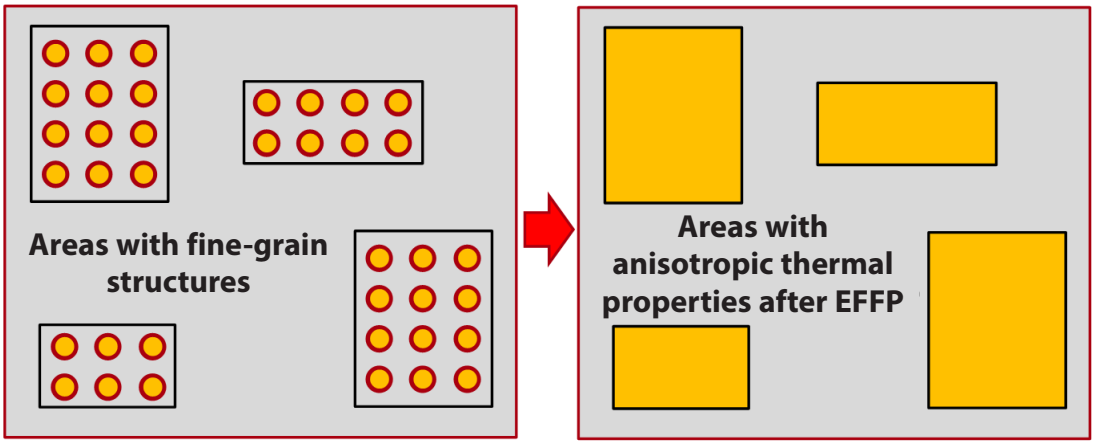

Figure 9: Effective Thermal Property Extraction (EFFP) reduces model complexity and accelerates simulations (image courtesy of CEA-Leti)

IPF support allows both gate and device-level power analysis to be used to construct fine-grain power maps needed to accurately capture hotspots on the die. Automatic compression of power sources in very high instance count designs, with source instances that run into millions, can be used to accelerate the simulation in FloTHERM.

Figure 10 shows the level of detail possible for a device having more than 150,000 fine grain structures including TSVs and µ-bumps, after simplification using EFFP and very complex BEOL with 9 metallization layers.

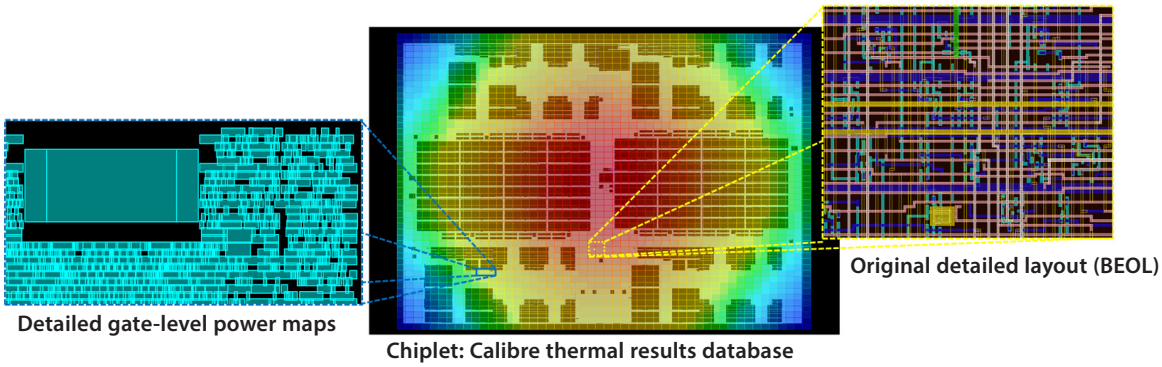

Figure 10: Detailed sign-off thermal analysis (image courtesy of CEA-Leti)

Finally, automatic constraint checks avoid error-prone and time-consuming manual verification of the thermal constraints. For the design shown in Figure 10 EFFP and smart power map conversion features reduced simulation time from many hours/days to less than an hour:

- Thermal property extraction (EFFP): **30 minutes** (once per thermal model)
- Power map generation from IPF: less than **2minutes** (once per application scenario)
- Thermal simulation of complete packaged 3D IC: **50 minutes**

CONCLUDING REMARKS

Package-centric approaches are no longer valid in advanced technologies and modern applications, mainly in advanced 3D ICs. FloTHERM integrated with Project Sahara is a powerful and flexible platform enabling:

- Detailed die-level thermal modeling compatible with advanced 3D integration technologies
- Complete chip-package-system thermal simulation with realistic boundary conditions
- Easy integration with standard ASIC design flows
- Accurate modeling of very complex designs using EFFP feature
- Thermal-aware 3D partitioning and early package co-design
- Sign-off thermal analysis of complex multi-die designs
- Rapid, detailed and accurate thermal assessment across the chip-package design flow

CEA-Leti [Ref 4, 5] describe the use of FloTHERM integrated with Project Sahara for a heterogeneous logic-on-logic 3D-Network-on-Chip asynchronous multicore device for a 4G telecom application, including DFT and fault tolerance in the design.

> "The implemented thermal model presents very good accuracy, the worst case difference between simulation and measured data is equal to 3.75% while the average difference considering all thermal sensors is lower than 2%."
>
> Dr Pascal Vivet, Research Engineer, CEA-Leti

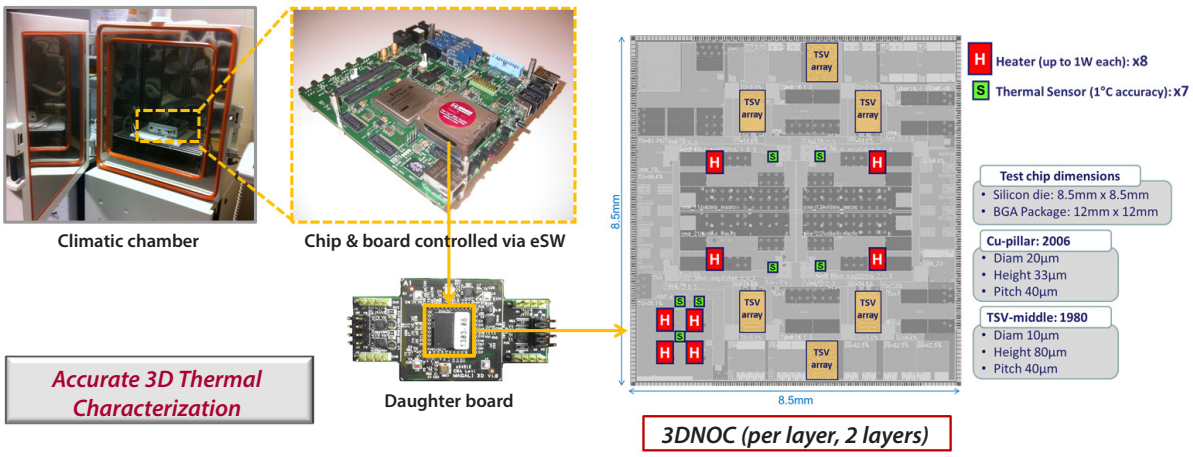

Figure 11: 3DNOC: experimental setup for thermal characterization (image courtesy of CEA-Leti)

ACKNOWLEDGEMENTS:

Byron Blackmore, FloTHERM Product Manager, Mentor
Pascal Vivet, Research Engineer, CEA-Leti

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

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